REMARKS

Claims 1-4, 6-11, 13, 16-29, 31, 33-35, 37 and 38 are in the application, with Claims 1, 3, 4, 7, 9, 13, 16, 18-20, 22, 25, 26, 27, 31, 33, 37 and 38 having been amended, with Claims 5, 6, 12, 14, 15, 30, 32 and 36 having been cancelled. Claims 1, 9, 16, 27 and 33 are the independent claims herein. No new matter has been added. Reconsideration and further examination are respectfully requested.

Objection to Drawings

Replacement sheets for FIGS. 4 and 6 are enclosed herewith for responding to the objection thereto. Withdrawal of the objection is respectfully requested.

Claim Objections

Claims 3-7, 12-14, 18-20, 22, 25, 30-32 and 36-38 were objected to due to informalities noted in the Office Action. The claims have been amended as shown above to change all references to "a (or the) supply voltage" to "an (the) output supply voltage" or "an (the) input supply voltage". Withdrawal of the objections is respectfully requested.

Claim Rejections

Claims 1-4, 7-14, 9-14, and 16-32 were rejected under 35 U.S.C. §102(a) as allegedly anticipated by U.S. Patent No. 6,566,848 (Horigan); Claims 1-32 were rejected under §102 as allegedly anticipated by U.S. Patent Application Publication No. 2004/0003310 (Hsu); and Claims 33-38 were rejected under 35 U.S.C. §103(a) over Hsu in view of Microsoft Computer Dictionary (Microsoft). Reconsideration and withdrawal of the rejections are respectfully requested.

Claims 1 and 16

Amended independent Claims 1 and 16 each relate to reception of a first signal from an integrated circuit. The first signal represents a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second

supply current value associated with the second supply voltage value. An output supply voltage is output to the integrated circuit based on the first signal. As described in the present specification, some embodiments of the foregoing enable a voltage regulator to provide power to an integrated circuit according to a load line specified by the integrated circuit.

The art of record is not seen to disclose or to suggest the foregoing features of Claims 1 and 16. Specifically, the art of record is not seen to disclose or to suggest reception of a first signal from an integrated circuit, wherein the first signal represents a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply voltage value.

Horigan describes a system to determine a load line for a microprocessor. Column 2, lines 46 through 49 and column 3, lines 5 through 7 indicate that a preset load line is initially set by external resistors. The preset load line may then be adjusted using stored data, as described at column 2, lines 50 through 58. FIG. 5 and column 3, lines 5 through 43 set forth a process to generate the data that is used to adjust the load line. The process includes measuring a low-load microprocessor current and a high-load microprocessor current through resistor 25. As described, the measured currents may be used to determine a new load line and offset voltage that are stored and used to adjust the preset load line.

Accordingly, nowhere does Horigan describe reception of a first signal from an integrated circuit, wherein the first signal represents a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply voltage value.

Hsu is also not seen to describe the features of Claims 1 and 16. Processor 201 of Hsu provides an IccID signal and a second, separate VccID signal to voltage regulator 210. The VccID signal indicates a supply voltage Vcc to be provided to processor 201 in a case that a supply current Icc = 0. The IccID signal indicates a maximum supply current Icc but does not indicate a voltage associated with the maximum supply current Icc. Accordingly, and as described at paragraph [0027], voltage regulator 210 must estimate a lower supply voltage limit 323 to which supply current Icc corresponds. Hsu therefore clearly does not describe reception

of a first signal from an integrated circuit, wherein the first signal represents a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply voltage value.

Independent Claims 1 and 16 are therefore believed to be allowable. Withdrawal of the rejections thereof is respectfully requested.

Claims 9 and 27

Amended independent Claims 9 and 27 each relate to transmission of a first signal from an integrated circuit to a voltage regulator. The first signal represents a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply voltage value. An input supply voltage having a value based on the first signal is then received from the voltage regulator. Some embodiments of the foregoing enable an integrated circuit to receive power from a voltage regulator according to a load line specified by the integrated circuit.

The art of record is not seen to disclose or to suggest the features of Claims 9 and 27, particularly with respect to transmission of a first signal from an integrated circuit to a voltage regulator, wherein the first signal represents a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply voltage value.

Horigan describes a system in which no associated supply voltage and supply current values are transmitted from an integrated circuit to a voltage regulator. Instead, Horigan determines a preset load line based on external resistor values. Horigan also describes adjusting the preset load line by measuring a low-load microprocessor current and a high-load microprocessor current through resistor 25.

Hsu describes a transmitting a signal indicating a supply voltage Vcc to be provided to processor 201 in a case that a supply current Icc = 0, and a separate IccID signal indicating a

maximum supply current Icc. Accordingly, neither Hsu nor Horigan describes reception of a first signal from an integrated circuit, wherein the first signal represents a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply voltage value.

Claims 9 and 27 are therefore believed to be in condition for allowance, and Applicants respectfully request withdrawal of the associated rejections.

Claim 33

Amended independent Claim 33 relates to a system including a microprocessor, a voltage regulator, and a double data rate memory. The microprocessor is to transmit a first signal representing a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply voltage value. The voltage regulator is to receive the first signal and to output an output supply voltage to the microprocessor based on the first signal, and the double data rate memory is electrically coupled to the microprocessor.

As described above, none of the art of record is seen to describe transmission by a microprocessor of a first signal representing a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply voltage value. Claim 33 is therefore believed to be allowable for at least the foregoing reasons.

CONCLUSION

The outstanding Office Action presents a number of characterizations regarding each of the applied references, some of which are not directly addressed herein because they are not related to the rejections of the independent claims. Applicants do not necessarily agree with the characterizations and reserve the right to further discuss those characterizations.

For at least the reasons given above, it is submitted that the entire application is in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience. Alternatively, if there remains any question regarding the present application or any of the cited references, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is cordially requested to contact the undersigned via telephone at (203) 972-0049.

Respectfully submitted,

September 29, 2006
Date

Nandu A. Talwalkar
Registration No. 41,339
Buckley, Maschoff & Talwalkar LLC
Attorneys for Intel Corporation
Five Elm Street
New Canaan, CT 06840
(203) 972-0049

attachments: Replacement Sheets for FIG. 4 and FIG. 6